DETAILED ACTION

Claim Objections

Comments of the Examiner

Claims 2 and 12 are objected to because of the following informalities:

Claim 2 recites the limitation "each charge conversion node" in line 4 of claim 2, which the examiner believes should read "each detection node."

Reply to the Examiner's Comments

Claim 2 has been amended to change "each charge conversion node" to -each detection node-.

Comments of the Examiner

Claim 12 is misnumbered. The examiner believes that claim 12 should be renumbered 11.

Reply to the Examiner's Comments

Claim 12 has been renumbered as Claim 11, and Cancelled.

Claim Rejections - 35 USC 102

Claims 1-3 and 9 have been rejected under 35 U.S.C. 102(b) as being anticipated by Kaplan (US Patent # 5,867,215).

Comments of the Examiner under the Rejection

In regard to claim 1, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture that incorporates charge multipliers (24), said image sensor including a first CCD register (14) adjacent to at least a second CCD register (16) and coupled to the said first register through a charge overflow barrier (22).

Reply to the Examiner's Comments

Kaplan's patent is not relevant, since it does not show anywhere charge multiplication CCD stages between the CCD wells 14,16.

FIG.1 clearly shows that (24) is an Amplifier, not a charge multiplier. The present invention shows CCD charge multiplication stages incorporated between the wells of the serial register. See FIG. 2a and 2b of the present invention. Charge is multiplied before it reaches the detection node.

While the structure may seemingly resemble the current invention, there are significant differences that need to be pointed out.

The Kaplan invention shows registers (14) located in the image sensing area (10) coupled to photo diodes (12). This is not the

case of the present invention where the registers are not located in the image sensing area and are not coupled to photo diodes.

The registers in Kaplan's invention, which are coupled to photo diodes (12) through gate (20) and barrier (22), transfer charge at once in parallel (vertical direction) from photo diodes to CCD wells (14) and the overflow charge to CCD wells (16). During the readout in the horizontal direction, charge is not transferred from one register to another, and moreover, it is not multiplied. Charge amount is not increasing during the readout and transfer from one CCD well (16) to another CCD well (16) and to the amplifier AMP (25). For this reason the wells in the Kaplan's patent have the same size. The anti-blooming overflow gate (31) is located on the other side (above) the photo diodes, not in any serial register.

In the present invention there are no photo diodes adjacent to registers. Charge is not supplied to registers in parallel (vertical) direction; charge is transferred in CCD registers in horizontal direction and register has charge multiplication stages incorporated between register wells. As the amount of transported charge increases due to the multiplication process, CCD wells need to be made wider to accommodate larger amount of charge. When

charge reaches the overflow area it overflows from one register to the other and further to an overflow drain while it is being transferred in the horizontal direction. This is not anticipated in the Kaplan's invention and any other referenced inventions, since there is no charge increase and the transfer of charge from one register to another is not expected during the horizontal charge transfer.

Comments of the Examiner under the Rejection

In regard to claim 2, note Kaplan discloses the use of that the second adjacent CCD register collects overflow charge (column 4, lines 33-39; the overflow charge is sent to the second CCD register, 16) and transports it to at least one detection node located in each register (column 4, lines 40-51; the transport of the signal from the CCD well to the amplifier is considered to be the equivalent of the detection node), and each detection node having charge conversion sensitivity that may be different for each node (column 5, lines 1-6; although not explicitly stated, it is inherent that the sensitivity changes with respect to the charge handling capabilities, and the CCD registers, 14 and 16, are of different charge handling capabilities).

Reply to the Examiner's Comments

In regard to claim 2: As explained above, in Kaplan's invention the overflow charge is transferred into the second register before sending it to the detection node. Charge is not transferred from one register to the other during the process of horizontal transfer to the detection node. As can be seen in FIG.3

of present invention, charge overflows from one register to the other due to one register being narrower and not being able to accommodate the transported charge. This feature is not explained in any of the cited references, Kaplan's Farrier's (US 6,392,260), and Burt's (US 6,444,968). In particular, the Burt's patent takes great pains in avoiding such overflows and shapes the wells accordingly so they will not overflow.

Comments of the Examiner under the Rejection

In regard to claim 3, note Kaplan discloses that the signals from adjacent register detection).nodes are processed and combined according to a predetermined mathematical formula (column 5, lines 45-61)

Reply to the Examiner's Comments

Present invention does not make such a claim.

Comments of the Examiner under the Rejection

In regard to claim 9, note Kaplan discloses the use of a solid-state image sensor (10) having a readout architecture, said readout architecture incorporating charge multipliers (24 and 26) CCD registers (14 and 16), and charge overflow device in at least one of its registers (22)

Reply to the Examiner's Comments

Kaplan's invention does not include anywhere in its structure charge multipliers (24 and 26) it uses only charge detectors with

Amplifiers (24 and 25). In Kaplan's invention, charge overflow structure is clearly different from the present invention. Charge cannot overflow from one register to another during the horizontal transport to detection node and amplifier one stage at the time. In particular, charge cannot overflow from one register to the other due to the intentional design of the smaller register well, which forces charge in one particular stage to overflow to the second register. In Kaplan's and Farriers's inventions, registers are purposely designed such that charge does not overflow during horizontal transport.

Claim Rejections -35 USC 103

Claims 4 and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Burt et al. (US Patent # 6,444,968) in view of Farrier et al. (US Patent # 6,392,260).

Comments of the Examiner under the Rejection

In regard to claim 4, note Burt discloses the use of a solid-state image sensor (2) having a readout architecture that incorporates charge multipliers (column 4, lines 55-64; and figure 1: 5 and 10), said image sensor including: a CCD register that incorporates at least one charge-multiplication device element in at least one stage (column 4, lines 55-64; and figure 1: 5 and 10). Therefore, it can be seen that the Burt device lacks the use of said at least one stage having a progressively wider width. Farrier discloses the use of a CCD register having a progressively wider width (column 7, line 66 column 8, line 28; and figure 3: 110).

Farrier teaches that the use of a progressively wider width is preferred in order to carry all the charge transferred without blooming (column 8, lines 25-28). Therefore, it would have been obvious to one of ordinary skill in the art to modify the Burt device to include the use of a progressively wider width as suggested by Farrier.

Comments of the Examiner under the Rejection

There is no mention of charge multiplier in Burt's (column 4 line 55). There are no charge multipliers in Burt's FIG.1: 5 and 10.

Comments of the Examiner under the Rejection

In regard to claim 8, note Burt discloses that the CCD register has a charge overflow barrier (16) and a charge overflow drain (17) incorporated in at least one of its stages to prevent charge blooming (column 6, lines 20-25).

Comments of the Examiner under the Rejection

Claim 8 has been cancelled

Rejection of Claims 7, 10 and 11 under 35 U.S.C. 103(a)

Claims 7, 10, and 11 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Burt et al. (US Patent # 6,444,968) in view of Earner et al. (US Patent # 6,392,260), and further in view of Applicant's admitted prior art.

Comments of the Examiner under the Rejection

In regard to claim 7, note the primary reference of Burt in view of Farrier discloses the use of a solid-state image sensor having a readout architecture as claimed in claim 4. Therefore, it can be seen that the Burt device lacks the use of a CCD register that includes a clearing gate and a clearing drain to remove unwanted charge. However, based on the Applicant's admission of prior art in the specification, the use of a CCD register that includes a clearing gate and a clearing drain to remove unwanted charge is well known and expected in the art (page 11, lines 1-7; Applicant also admits that this feature is not essential to the function of the invention). Therefore, it would have been obvious to one of ordinary skill in the art to modify the primary device to include the use of a CCD register that includes a clearing gate and a clearing drain to remove unwanted charge as suggested by Applicant.

In regard to claim 10, note the primary reference of Burt in view of Farrier discloses the use of a solid-state image sensor having a readout architecture as claimed in claim 4. Therefore, it can be seen that the Burt device lacks the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise. However, based on the Applicant's admission of prior art in the specification, the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise is well known and expected in the art (page 4, lines 16- 20: "However, in most CCD registers, the high field and the injection of electrons progresses along the length of the register"). Therefore, it would have been obvious to one of ordinary skill in the art to modify the primary device to include the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise as suggested by Applicant.

In regard to claim 11 (numbered 12), note the primary reference of Burt in view of Farrier discloses the use of a solid-state image sensor having a readout architecture as claimed in claim 4. Therefore, it can be seen that the Burt device lacks the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate, and wherein the charge flows in said one direction through a high electrical field to minimize charge multiplication noise. However, based on the Applicant's admission of prior art in the specification, the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate wherein charge flows in that one direction through a high electrical field to minimize charge multiplication pulse amplitude is well known and expected in the art (page 4, lines 16- 20: "However, in most CCD registers, the high field and the injection of electrons progresses along the length of the register"). Therefore, it would have been obvious to one of ordinary skill in the art to modify the primary device to include the use of a sensor that is oriented in a one crystallographic direction on the semiconductor substrate wherein charge flows in that one direction through a high electrical field to minimize charge multiplication pulse amplitude as suggested by Applicant.

Reply to the Examiner's Comments

Claims 7 10 and 11 (previously 12) have been cancelled.

Allowable Subject Matter

Reply to the Examiner's Comments

Claims 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As for claims 5, the prior art does not teach or fairly suggest the use of a solidstate image sensor having a readout architecture having a CCD register having a progressively wider width, wherein the width of the register and the number of charge multiplication elements varies according to a predetermined formula.

Reply to the Examiner's Comments

Since it has been shown that Claim 1 is patentable over the cited prior art, there is no need to rewrite claims 5 and 6 at this time.

Reply to the Examiner's Comments

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US005337340A: note the use of charge multiplication elements in a CCD register.

US005652442A: note the use of CCD register with a charge boundary.

US004873561: note the use of a CCD register with antiblooming structure.

Reply to the Examiner's Comments

The above cited prior art has been reviewed, but nothing was found therein to render the claims of the present application unpatentable.

Summary

Since it has been shown that the Claims 1-6, and 9 (Claim 1 as amended) are patentable over the prior art, claims 7, 8 and 10 have been cancelled, it is respectfully requested that Claims 1-6 and 9 be allowed, and the application passed to issue.

Respectfully submitted,

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